Mô hình hóa điện áp đóng ngắt và giải thuật PWM cho biến tần đa bậc trong điều kiện nguồn không cân

Switching Voltage Modeling And PWM Control For Multilevel Inverters Under DC Voltage Unbalance

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Tóm tắt

Trong bài báo này, một mô hình điện áp đóng ngắt mới và giải biến điều biến dựa trên hàm offset cho biến tần đa bậc trong điều kiện nguồn không cân được trình bày. Mô hình điện áp đóng ngắt được mô tả chung cho hai cấu hình NPC và Cascade của biến tần đa bậc. Việc khảo sát điện áp mong muốn từ các thành phần điện áp đóng ngắt tích cực và không tích cực trong hệ tọa độ abc giúp thực thi việc điều khiển điện áp trong điều kiện nguồn không cân. Điện áp Offset được đưa ra như một biến điều khiển quan trọng trong mô hình điện áp đóng ngắt của biến tần đa bậc. Giải thuật PWM được điều khiển thông qua việc thiết kế hai thành phần Offset. Một điện áp Offset chính thiết kế dựa trên điện áp Common-mode yêu cầu, trong khi thành phần Offset thứ hai được giới hạn tính ảnh hưởng đến chất lượng PWM trong các cell điện áp. Chất lượng PWM được cải tiến để giảm tổn hao đóng ngắt bằng chế độ PWM gián đoạn-thông qua việc điều khiển điện áp Offset cục bộ theo dòng điện. Tính khả thi của giải thuật đề xuất được kiểm chứng bằng kết quả thực nghiệm.

Từ khóa: Kĩ thuật PWM, điện áp đóng ngắt, điều khiển Offset, điều kiện nguồn không cân, biến tần đa bậc.

Abstract: In this paper, a novel switching voltage modeling and offset-based Pulse Width Modulation (PWM) scheme for multilevel inverters with unbalanced dc sources is presented. The switching voltage model under DC-voltage imbalance will be formulated in general form for both Neutral point Clamped and cascaded multilevel inverter topologies. An analysis of the reference switching voltages from its active and non-active switching voltage components in *abc* coordinates can enable the voltage implementing for the unbalanced dc source condition. The offset voltage is introduced as an indispensable variable in the switching voltage model for multilevel voltage source inverters. The PWM performance is controlled through the design of two offset components in a subsequence. One main offset may refer to the common mode voltage, while the second offset restricts its effect on the quality of PWM control in related dc levels. An improving of the PWM quality as reduction of the switching loss in Discontinuous PWM mode can be obtained by setting the local offset related to the load currents. The validity of the proposed algorithm was verified by experimental results.

Keywords: PWM technique, switching voltage, Decoupling offset, Unbalance dc sources, Multilevel inverter.

1. Introduction

Multilevel inverters play an important role in current high performance applications. Two topologies have become especially popular: the neutral point clamped multilevel inverter and the cascaded multilevel inverter. A circuit diagram of a five-level NPC inverter is shown in Fig. 1. Well-known PWM methods include carrier-based (CPWM) and space vector (SVPWM) techniques [1]-[8]. Carrier-based PWM techniques are commonly used in practical applications because of their simple implementation. In a recent study, a novel carrier PWM method offered flexible control of vector redundancies in an offset generator [4]. The researchers showed that the algorithms of a space vector PWM scheme with the nearest three voltage vectors (NTV) can be completely realized by a

corresponding carrier PWM method

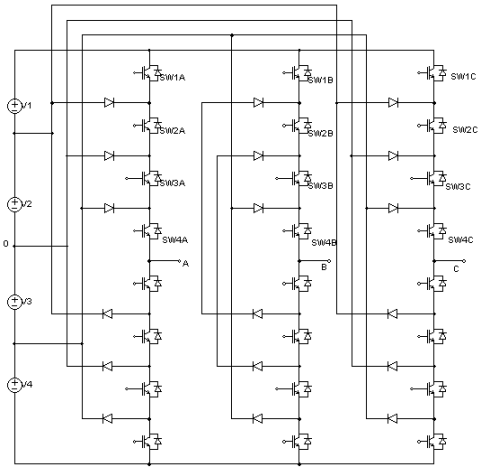

Fig. 1. Circuit of 5-level NPC inverter and defined switches.

The offset feature in a two-level inverter has been extensively investigated in previous studies [9]-[11]. Offset control is also available in space vector modulation by redistributing the switching time duties of the two redundant states [10]-[13]. Space vector PWM control is more sophisticated in a multilevel inverter [14], [15]. After determining the three pivot vectors, up to four active switching states can be selected. The algorithm may be difficult if the offset is used as a variable to control the dc neutral currents and thus, balance the dc voltages and reduce the impact of the common mode voltage (CMV) on the electrical drives [16], [17, [18]. The feed-forward compensating algorithm modified either the modulating signals or the carrier waves. More results can be found in other works where the PWM algorithm for balanced dc sources [19]- [22] and the feed-forward PWM algorithm for unbalanced dc sources [23] were separately solved. These studies were mainly reduced to an algorithm for computing the switching time duties for a previously defined reference. In later works [19], [21]-[23], a sinusoidal reference was assumed and the offset voltage was fixed as a constant. The modulation index was also limited to a value below 0.866 for balanced dc sources. In comparison with the conventional sinusoidal PWM technique, these methods were not convincing for their contribution to improving the PWM quality. Because of relying on the use of the redundant states, the loss of the vector redundancy under the dc voltage imbalance prevents this algorithm from the application. The offset voltage has been proven to have a large impact on converter performance. Proper offset voltage selection can reduce the number of switching and the harmonic distortion factor in different PWM techniques [4], [24]; its regulation with load currents may help to minimize switching loss [25]. Offset adjusting can generate different PWM modes [3], [26]. Therefore, the offset voltage is practically indispensable and an important variable in the control model of a multilevel voltage source inverter.

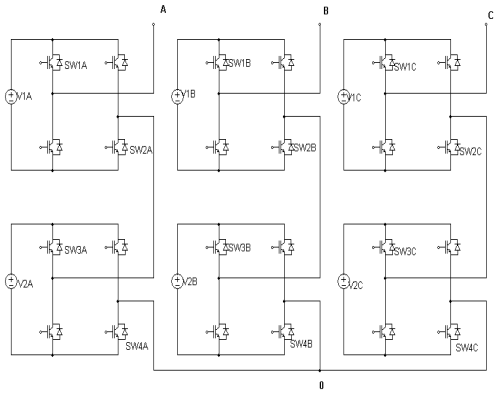

Fig. 2. Circuit of 5-level cascaded inverter and defined switches

Several offset functions have been introduced in previous research [1], [3], [26]-[31]. However, each PWM method had its own algorithm and was available for some particular demand.

In this paper, a novel approach of modeling the switching voltages and offset-based PWM scheme for multilevel inverter in *abc* coordinates is proposed. Its main contributions are clarified in the following points:

Control characteristics of multilevel inverters are described through the switching voltages. Formulation and implementation of the switching voltages strictly relate to the offset design.

Offset based PWM quality control: in the proposed PWM scheme, the global offset enables controlling draft common mode voltage and the local offset to set PWM modes such as for reduction of switching loss.

General applicability: The proposed method introduces a unified and offset based feed-forward PWM control that is applicable to both NPC and cascaded multilevel inverters of any number of levels.

The validity of the proposed feed-forward PWM method will be demonstrated with simulated and experimental results.

2. Switching voltage formulation for multilevel inverters under input voltage unbalance.

Due to the difference in structure of the diode clamped inverter and cascade inverter, as illustrated in Fig. 1 for five-level inverter, established rules of switching combinations for a same reference output voltage are different. In this paper, the analytical process for the two topologies can be unified by a simple voltage modeling.

2.1 Modeling of the switching voltage for NPC multilevel inverter

With selected neutral point 'O' and designated switches of X-phase represented as $SW_{1X}, SW_{2X}, SW_{3X}, SW_{4X}$ for the NPC topology in Fig. 1.

The pole leg voltage V_{X0} , (X=A,B,C) is determined as

$$v_{X0} = S_{1X}V_1 + S_{2X}V_2 + S_{3X}V_3 + S_{4X}V_4 - V_3 - V_4 \quad (1)$$

where $S_{1X}, S_{2X}, S_{3X}, S_{4X}$ represent the switching states of $SW_{1X}, SW_{2X}, SW_{3X}, SW_{4X}$ respectively, s_{1A} is '1' if SW_{1A} is ON, otherwise its value is '0'.

We define the X-phase switching voltage V_{SX}, (X=A,B,C) that is controlled by switches as :

$$V_{SX} = \sum_{j=1}^{n-1} V_{SXj} = \sum_{j=1}^{n-1} S_{jX} V_{jX} \quad (2)$$

The switching voltage presents a switching controlled voltage source to supply the load. From (2), the switching voltage consists of (n-1) switching voltage components. The j-th switch voltage is defined as a product of the j-th switch state and the corresponding DC voltage cell:

$$V_{SXj} = S_{jX} V_{jX} \quad (3)$$

During a sampling period, for the X-phase inverter leg, X=A,B,C, the only one switch is actively turn on and off and called *the active switch* S_X. The remaining (n-2) switches have their states unchanged ($S_{jX} = 1$ or $S_{jX} = 0$) and called *the non-active switches*. The non-active switch provides a full voltage of $V_{SXj} = V_{jX}$ for $S_{jX} = 1$ and zero voltage of $V_{SXj} = 0$ for $S_{jX} = 0$. Among (n-2) non-active switches, we suppose there are L switches to hold ON-state and (n-2-L) switches to hold OFF state. We define V_{LX} the value of the non-active switching voltage provided by the non-active switches. For the active switch S_X, we define ξ_X be a duty cycle and V_{DCX} be the DC-voltage linked with this active switch. We obtain instantaneous and average values of the switching voltages in the form of its components – the non-active switching voltage and the active switching voltage as:

$$V_{SX} = V_{LX} + S_X V_{DCX} \quad (4)$$

$$\overline{V}_{SX} = V_{LX} + \xi_X V_{DCX} = V_{LX} + e_X \quad (5)$$

The relation between the switching voltage $\overline{V}_{SX}$, the non-active switching voltage V_{LX} and the DC-voltage linked to the active- switch V_{DCX} can be described as:

$$V_{LX} \le \overline{V}_{SX} \le V_{LX} + V_{DCX} \quad (6a)$$

The constraint between switch states for 5-level NPC inverter shown in Fig.1 is simply expressed as

$$0 \le S_{1X} \le S_{2X} \le S_{3X} \le S_{4X} \le 1 \quad (6b)$$

In order to formulate the switching voltage in relation to the fundamental voltage, let's analyze the phase to pole voltage v_{X0} in relation to its non-zero and zero sequence voltage as:

$$v_{X0} = V_{X1} + V_{off} \quad (7)$$

where

$$V_{A1} = \frac{2V_{A0} - V_{B0} - V_{C0}}{3}; \; V_{B1} = \frac{2V_{B0} - V_{C0} - V_{A0}}{3}$$

$$V_{C1} = \frac{2V_{C0} - V_{A0} - V_{B0}}{3}; \; V_{0ff} = \frac{V_{A0} + V_{B0} + V_{C0}}{3}$$

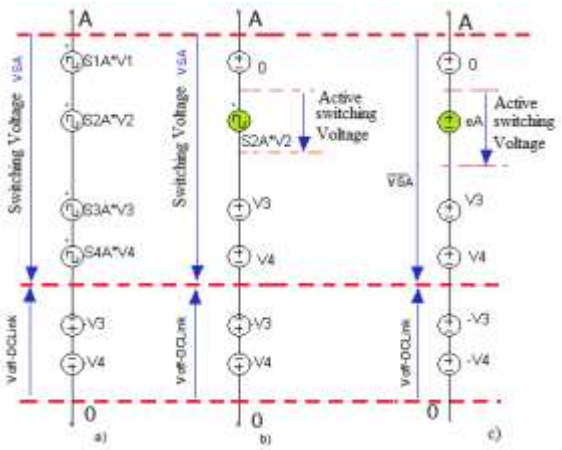

Fig. 3. a) Relation between the switching voltage and phase to neutral point voltage; b) A-phase switching voltage for non-active switches S1A=0; S3A=1;S4A=1; and active switch S2A; c) Average voltage model of the A-phase switching voltage.

We can see from (2), that the voltage V_{DCLink}, produced by DC-Link voltage connection (V3+V4) presents an offset voltage, termed $V_{off-DCLink}$:

$$V_{DCLink} = V_{off-Dclink} = V_3 + V_4 \quad (8)$$

Finally, we formulate the average switching voltages in sampling period as (10):

$$V_{SX} = V_{X1} + V_{off} + V_{off-DClink} \quad (9)$$

$$\overline{V}_{SX} = V^*_{X1} + V^*_{off} + V_{off-DClink} \quad (10)$$

where V^*_{X1} and V^*_{off} are the reference fundamental common mode voltages to satisfy:

$$\overline{V}_{X0} = V^*_{X1} + V^*_{off} \quad (11)$$

Equation (10) formulates the switching voltages of NPC multilevel inverter. The switching voltage model

for a single leg in relationship with the phase-to-pole voltage is presented in Fig.3 and for three phases in Fig.4. The brief form of switching voltage modeling is shown for a single phase in Fig.5 and for three phases in Fig.6.

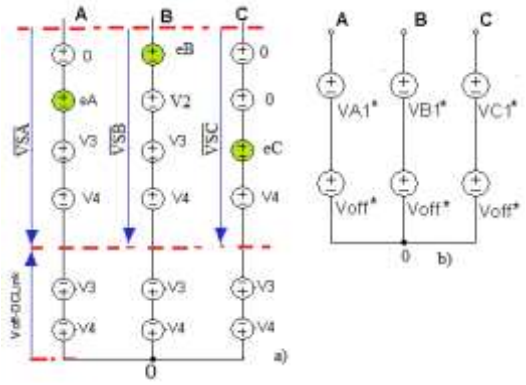

Fig. 4. Average voltage model of the three phase to pole voltages VA0,VB0,VC0 for active switches S2A, S1B and S3C consisting of : a) the switching voltages VSA,VSB,VSC and the DC-link voltage; and b) the fundamental voltages and the zero sequence voltage.

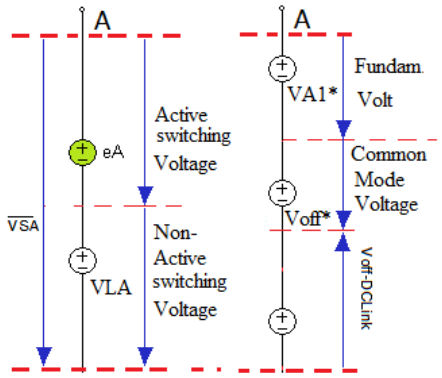

Fig.5. NPC inverter-A brief description of the A-phase switching voltage: (a) from the active and non-active Switching voltage components and (b) from zero/non-zero sequence voltages.

DC-link voltage injects a zero sequence voltage to the switching voltage. In other words, the switching voltages will provide both the fundamental voltages V_{X1}^{*}, the required common-mode voltage V_{off}^{*} and the zero sequence voltage injected from DC-link voltages.

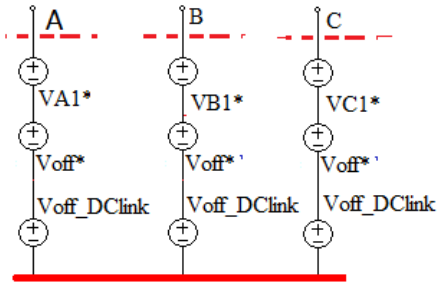

Fig. 6. General voltage model of three phase switching voltages $\overline{V}_{SA},\overline{V}_{SB},\overline{V}_{SC}$ for NPC inverter under DC-voltage imbalance

2.2 Modeling of the switching voltage for cascaded multilevel inverter

The switching voltage in the cascade inverter can be in principle explained for 3-level inverter as shown in Fig.7. The phase-to-pole voltage v_{A0} can be expressed as:

$$v_{A0} = V_{S1A} - V_{1A} + V_{S2A} = S_{1A}V_{1A} + S_{2A}V_{1A} - V_{1A} = V_{SA} - V_{1A}$$

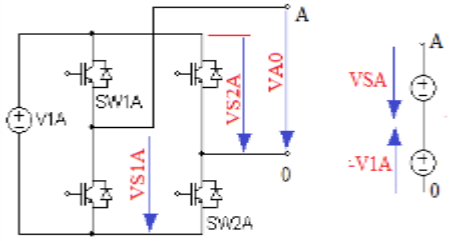

Fig.7: Relation between the switching voltage VSA, switch voltages VS1A, VS2A and the phase to pole voltage for 3-level cascaded inverter.

The switching voltage v_{SA} is the sum of two switching voltages v_{S1A} and v_{S2A}. Similarly, for 5-level cascade inverter as shown in Fig.2 and Fig.8, we obtain: (It should be noting that $s_{1X}, s_{2X}, s_{3X}, s_{4X}$ can be selected randomly in the five level cascaded inverter)

$$v_{X0} = S_{1X}V_{1X} + S_{2X}V_{1X} + S_{3X}V_{2X} + S_{4X}V_{2X} - V_{1X} - V_{2X} \quad (12)$$

For cascaded inverter, the constrain (6b) is not required.

From (8) and (12), the switching voltage at any instant can be deduced as (13)-(14):

$$v_{SX} = V_{X1} + V_{off} + V_{1X} + V_{2X} \quad (13)$$

for 5-level inverter, or in the relation with the non-zero and zero sequence voltages as:

$$v_{SX} = V_{X1} + V_{off} + V_{X1-Dclink} + V_{off-Dclink} \quad (14)$$

where:

$$v_{A1-Dclink} = \frac{1}{3}[2(V_{1A} + V_{2A}) - (V_{1B} + V_{2B}) - (V_{1C} + V_{2C})]$$

$$v_{B1-Dclink} = \frac{1}{3}[2(V_{1B}+V_{2B})-(V_{1C}+V_{2C})-(V_{1A}+V_{2A})] \quad (15)$$

$$v_{C1-dclink} = \frac{1}{3}[2(V_{1C}+V_{2C})-(V_{1A}+V_{2A})-(V_{1B}+V_{2B})]$$

$$v_{off-Dclink} = \frac{1}{3}\sum_{X=A,B,C}(V_{1X}+V_{2X}) \quad (16)$$

Using a similar approach to the NPC inverter, the switching voltage modeling for cascade inverter can be deduced in a sampling period as:

$$\bar{v}_{SX} = V_{X1}^{*} + V_{off}^{*} + V_{1X} + V_{2X} \quad (18)$$

Or in another form as:

$$\bar{v}_{SX} = V_{X1}^{*} + V_{off}^{*} + V_{X1-Dclink} + V_{off-Dclink} \quad (19)$$

Being different from the NPC inverter, the DC-link voltages in cascade inverter inject both non-zero sequence voltage component $V_{X1-Dclink}$ and zero-sequence voltage component $V_{off-Dclink}$ to the switching leg voltage. The non-zero sequence component will influence on the voltage control limit of the cascade inverter. The switching voltages in cascaded inverter have to provide both the fundamental voltages V_{X1}^{*}, and the non-zero sequence $V_{X1-Dclink}$ injected by the dc-link voltages. This problem presents a main difference compared to the NPC inverter.

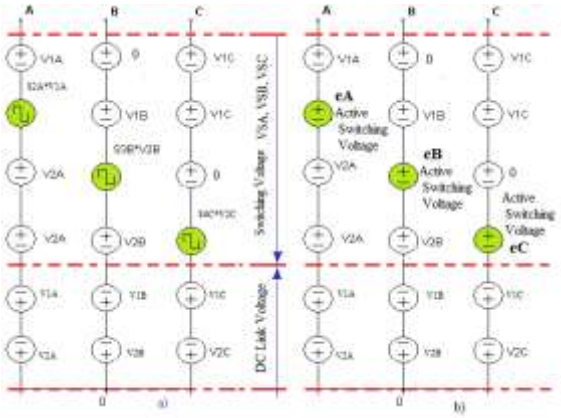

Fig.8. Voltage model of switching voltages and phase-to-pole voltage for 5-level cascaded inverter for active switches S2A, S3B and S4C; b) Average voltage model

The modeling of the switching voltage in cascaded inverter under DC voltage imbalance described above are drawn for single phase in Fig.9 and for three phases in Fig.10.

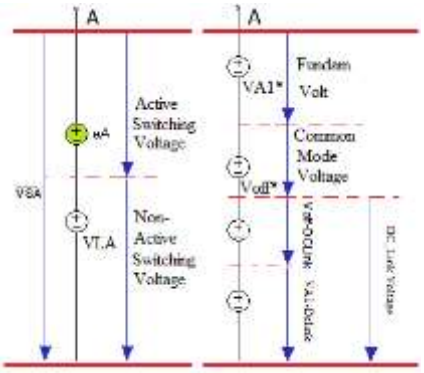

Fig. 9. Analysis of the A-phase switching voltage of cascaded inverter.

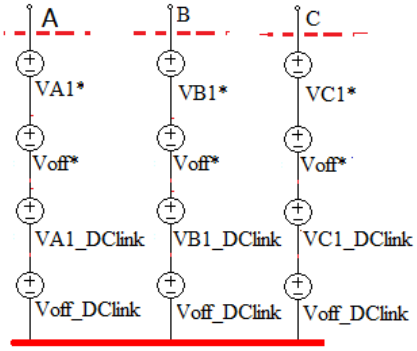

Fig.10. General voltage model of three phase switching voltages $\bar{V}_{SA}, \bar{V}_{SB}, \bar{V}_{SC}$ for cascaded inverter under DC-voltage imbalance

2.3 The fundamental voltage limit

In order to describe completely the switching voltage model, two parameters must be determined: (a) the reference fundamental voltage and (b) the common mode voltage. Answering will be clear if these voltage limits are determined.

The maximum (or minimum) value of the switching voltage will be obtained if all the switches are "ON" (or "OFF").

For NPC inverter, it can be deduced as:

$$V_{SWMAX} = V_{SAMAX} = V_{SBMAX} = V_{SCMAX} = V_1 + V_2 + V_3 + V_4 \quad (20)$$

$$V_{SWMIN} = V_{SAMIN} = V_{SBMIN} = V_{SCMIN} = 0 \quad (21)$$

Because the three inverter legs have the same DC-link voltages, the voltage vectors at the boundary form a symmetrical hexagonal diagram as shown in Fig.11a. The DC-voltage imbalance in the DC-link doesn't influence on the voltage limit in under-modulation of the NPC inverter. We then can obtain the maximum fundamental voltage V_{X1}^{*} of the under-

modulation limit as follows:

$$V^*_{1MAX} = \frac{V_{SWMX}}{\sqrt{3}} \quad (22)$$

For cascaded inverter, the limits of the switching voltages will be

$$V_{SAMAX} = 2(V_{1A} + V_{2A});\ V_{SBMAX} = 2(V_{1B} + V_{2B});$$
$$V_{SCMAX} = 2(V_{1C} + V_{2C}) \quad (23)$$

$$V_{SAMIN} = V_{SBMIN} = V_{SCMIN} = 0 \quad (24)$$

For cascade inverter, because the three inverter legs have different DC-link voltages, the voltage vectors at the boundary form an unsymmetrical hexagonal diagram as shown in Fig.11b. The maximum fundamental voltage amplitude in under-modulation range V^*_{1MAX} for cascaded inverter is equal to the smallest amplitude of the voltage vector that lying on the outmost boundary. The value of V^*_{1MAX} is obviously reduced with the increasing imbalance of dc-link voltage and determined from the two lower switching voltages V_{SWMN}, V_{SWMD}, defined as:

$$V^*_{1MAX} = \frac{V_{SWMN} + V_{SWMD}}{2\sqrt{3}} \quad (25)$$

where

$$V_{SWMD} = Mid[V_{SAMAX}, V_{SBMAX}, V_{SCMAX}] \quad (26)$$
$$V_{SWMN} = Min[V_{SAMAX}, V_{SBMAX}, V_{SCMAX}]$$

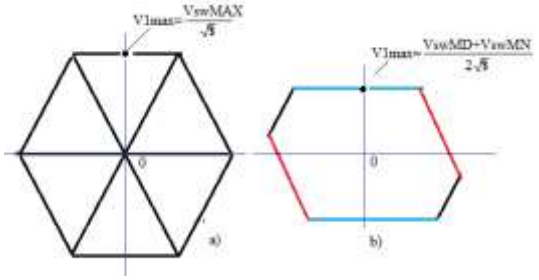

Fig.11. Limit boundaries of the voltage vector diagram for multilevel inverter under dc-voltage imbalance: a) for NPC inverter; b) for cascaded inverter.

2.4 The common mode voltage limit- the global offset v_{off}

The second required parameter in the switching voltage formulation (10) and (19) is the common mode voltage V^*_{off}. In general, this global offset can be expressed as a function of variable η_1 as:

$$v^*_{off} = \eta v_{off-MX} + (1-\eta) v_{off-MN};\ 0 \le \eta \le 1 \quad (27)$$

Where the maximum and minimum global offset can be deduced for NPC inverter as:

$$V_{off-MX} = [Min(V_{SWMAX} - V^*_{X1}) - V_{off-Dclink}],\ \text{X=A,B,C} \quad (28)$$

$$V_{off-MN} = [-Min(V^*_{X1}) - V_{off-Dclink}],\ \text{X=A,B,C}$$

and for the cascaded inverter:

$$V_{off-MX} = Min(\frac{V_{SXMAX}}{2} - V^*_{X1}),\ \text{X=A,B,C} \quad (29)$$

$$V_{off-MN} = -Min(\frac{V_{SXMAX}}{2} + V^*_{X1}),\ \text{X=A,B,C}$$

Function "Min" selects the smallest value of the function from three phase (A,B,C) function values.

Medium common mode voltage [9]-[12]: This common mode voltage approach is commonly used in two-level inverter and multilevel inverter to maximize the linear PWM control range. For it, the global offset is defined by setting $\eta_1 = 0.5$ in (30) as follows:

$$v_{off-Med} = (v_{off-MX} + v_{off-MN})/2. \quad (31)$$

Minimum common mode voltage: The resulting sinusoidal PWM method is a particular case of this PWM technique (with $v_{off-Opt} = 0$) for a modulation index range lower than 0.866:

$$v_{off\text{-}Opt} = \begin{cases} v_{off\text{-}MX} & \text{if } v_{off\text{-}MN} \le v_{off\text{-}MX} \le v_{off\text{-}Opt} \\ v_{off\text{-}MN} & \text{if } v_{off\text{-}Opt} \le v_{off\text{-}MN} \le v_{off\text{-}MX} \\ v_{off\text{-}Opt} & \text{if else} \end{cases} \quad (32)$$

From (24),(25),(28) and (29), the utmost voltage limits of the switching voltages do not depend on the voltage difference between the DC-link voltages in each phase, but depending on the difference of total DC-link voltages between three phases. As results, only in the cascaded inverter, the control voltage capability will be influenced by DC-link voltage imbalance.

3. Switching voltage implementation

3.1 Switching voltage PWM Control

The three-phase switching voltage formulated for NPC and cascaded inverter by (10) and (19) and shown in Fig.6 and Fig.10, can be now implemented by a unified PWM control algorithm. For this aim, the switching voltage will be considered as a sum of the active and non-active switching voltages as shown in Fig.12a. A transfer to modulating signal model is given in Fig.12b.

For the active switches, their switching state sequence can be realized by carrier based PWM approach illustrated in Fig.13 with the modulating

signals ξ_X , X=A,B,C calculated as:

$$\xi_X = \frac{\bar{V}_{SX} - V_{LX}}{V_{DCX}} \qquad (33)$$

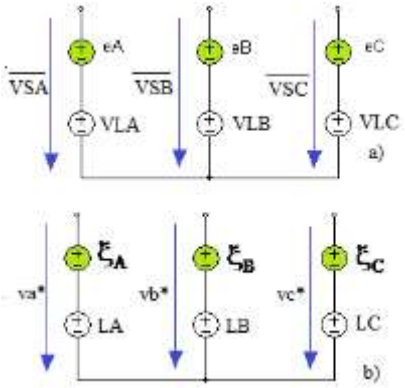

Fig.12. a) Voltage model of the switching voltage for implementation; b) Modulating signal model in carrier based PWM.

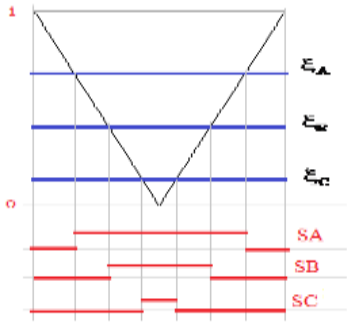

Fig.13. Switching time diagram for implementing the active switching voltages

The non-active voltage V_{LX} restricted by (6a) is defined as the nearest and not exceed the switching voltage $\bar{V}_{SX}$. For NPC inverter, for given switching voltages and DC-link voltages, the states of the non-active switches can be determined by conditions (6a) and (6b). As result, the active switch and related DC linked voltage and duty cycle can be deduced as (33). For cascaded inverter, the condition (6b) is not required. Because the role of each switch in the switching voltage (2) is similar, for example, a periodical alternating of switch combinations can be set for balancing the switching loss between the devices. For each combination, the DC-link voltage of cascaded inverter will become "fixed" similar in NPC inverter and the switch condition (6a) may apply to the new arranged DC voltages. Then the PWM control algorithm can be unifed for both cascaded and NPC inverter.

Eight switching states of the active switches establish a voltage vector diagram as shown in Fig.14. Each voltage vector is calculated as

$$\vec{E} = \frac{2}{3}(S_A V_{DA} + S_B V_{DB} e^{j120} + S_C V_{DC} e^{j240}) \qquad (34)$$

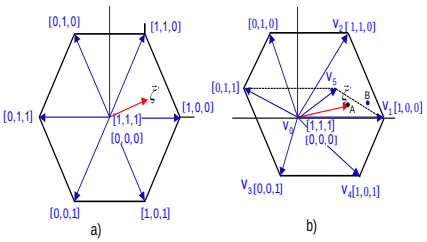

Fig. 14. Vector diagram of the active switching voltages for (a) balanced dc sources and (b) unbalanced dc sources. $V_{DA} > V_{DB} > V_{DC}$

The active switching voltage vector diagram has similar characteristics for both the cascade and NPC inverters. It forms an unsymmetrical hexagon. Obviously, the only zero vector of switching state (000) is located at the center. The vector of switching state (111) is located out of the center, different with (000). Unbalanced DC voltages can make the hexagon to be much distorted. As results of these things, for example, for the reference vector in Fig.14b, the PWM control with three nearest vector principle cannot be implemented with the minimized switching number. As a result, an optimizing total harmonic distortion factor may not be always gained with conventional PD, POD PWM techniques. For example, the reference voltage in Fig.14b is positioned in the triangle of three nearest vectors (000), (100) and (111), which cannot be realized with any from mentioned PWM techniques. Another disadvantage is that the transfer from continuous PWM mode to discontinuous PWM mode by simly deleting the switching state (000) or (111) from PWM pattern is generally not allowed. This is because, under DC voltage imbalance, the transfer required the offset change may produce different middle switching states in the switching sequence. For example, the switching state sequence of continuous PWM (000)-(100)-(101)-(111) after removing the state (111) cannot implement the reference voltage vector in Fig.14b, because the remaining state (000)-(100)-(101) do not contain the reference in their limited area.

3.2 Active switching voltage control – Designing of the local offset for reduced switching loss

From the voltage model of multilevel inverter shown in Fig 12a, a further improving of the PWM performance can be done by modifying the active switching voltages. In this part, the control is

provided with adding termed a local offset voltage e0 to the current active voltages as shown in Fig.15.

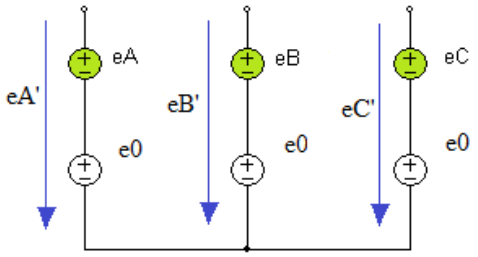

Fig.15. Modified PWM control of the active switch voltage by adding the local offset voltage

$$e_X^{'} = e_X + e_0 = \xi_X^{'} V_{DX}\ ;\ X = A,B,C \quad (35)$$

The modulating signals will be modified as:

$$\xi_X^{'} = \frac{e_X + e_0}{V_{DX}} \quad (36)$$

Reduced switching loss PWM under DC voltage imbalance:

The local offset e_0 range is dependent on the reference local leg voltage and the three active dc-cells. It can be varied in the following range (see Fig. 4a):

$$e_{0MN} \le e_0 \le e_{0MX} \quad (37)$$

The resulting reference leg voltages of the virtual two-level inverter can be expressed as follows:

$$e_{0MX} = Min(V_{DA} - e_A, V_{DB} - e_B, V_{DC} - e_C) \quad (38)$$

$$e_{0MN} = -Min(e_A, e_B, e_C) \quad (39)$$

From (37-39), the local offset can be expressed as a function of variable η_2, as follows:

$$e_0 = (1-\eta_2)e_{0MN} + \eta_2 e_{0MX}\ ;\quad 0 \le \eta_2 \le 1 \quad (40)$$

For example, a discontinuous PWM method can be obtained if the value of the parameter η_2 is set equal to 1 or 0. We define X-phase and Y-phase, which are available to discontinuous PWM, by adding corresponding to e_{0MX} and e_{0MN} to the active switching voltages e_X.

We define IMX, and IMD are their maximum and medium absolute currents from 3 –phase currents i_A, i_B, i_C. The selection rule of e_0 for reduced switching loss can be found as $X = A,B,C$, $Y = A,B,C$

$$e_0 = \begin{cases} e_{0MX} & i_X = I_{MX} \quad OR \quad i_X \ne I_{MX}; i_Y \ne I_{MX}; i_X = I_{MD} \\ e_{0MN} & i_Y = I_{MX} \quad OR \quad i_X \ne I_{MX}; i_Y \ne I_{MX}; i_Y = I_{MD} \end{cases} \quad (41)$$

The conventional SVPWM method can also be approximately extended to a multilevel inverter by setting the parameter $\eta_2 = 0.5$ in (40) as follows:

$$e_0 = \frac{e_{0MX} + e_{0MN}}{2} \quad (42)$$

For a small level of unbalanced dc sources, (42) would satisfy for a low current ripple in the entire modulation index.

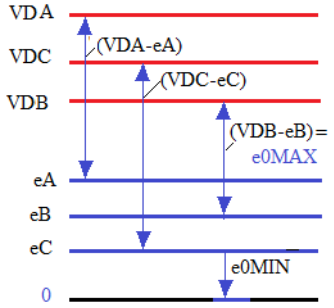

Fig. 16. Determination of the local offset limits from the active voltages and related DC-link voltages

3.3 PWM Control scheme

The PWM control scheme for both NPC and cascade multilevel inverters under the DC-voltage imbalance is drawn in Fig.17. In this scheme, there are three main block function functions.

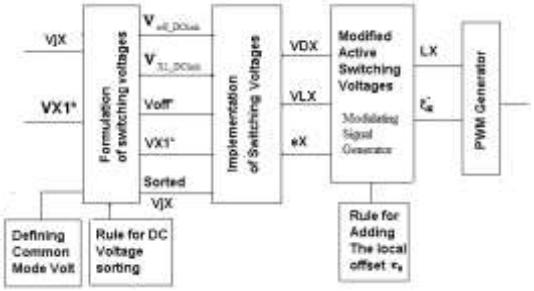

Fig. 17. Proposed PWM Control scheme for multilevel inverter under condition of DC-voltage imbalance.

The first block presents the formulation of the switching voltages. The only variable can be proposed in this stage is the common mode voltage function. Block "Rule of DC-voltage sorting" is applied only for the cascade multilevel inverter topology. Block "Implementation of the switching voltage" decomposes the switching voltage into the active and non-active switching voltage components. The another block "Modified active switching voltage" will design the local offset voltage for an improving the PWM performance. The resulted active voltages and non-active switching voltages will be used to generate the modulating signals at its outputs. They are put as inputs for carrier based PWM generator in

the final block.

4. Experimental results

Experimental hardware was built for the three-level NPC inverter so as to validate the proposed theory. The algorithm is implemented using the eZdsp TMS320F2812 control kit. Two DC voltages were measured with LEM LV25 NP Hall sensors and filtered through a low pass filter with a cut-off frequency of 1 kHz.

The current sensors Hall LEM LA25NP were used to measured phase load currents. The frequency of the triangle carrier waveform was set at 5 kHz. The experimental parameters were $v_{C1} = 50V$, $v_{C2} = 70V$, $f_0 = 50Hz$, $R = 10\text{W}$ and $L = 60mH$.

Without compensation: The PWM algorithms without compensation were gradually realized with m = 0.3 and 0.8. The phase load voltage, currents, and FFT diagrams of the current without compensation for m = 0.3 are shown in Fig. 18(a), respectively. The low-order harmonics, particularly the second-order harmonic, were rejected from the output current after the compensating algorithm was applied. The load voltage, currents, and FFT diagrams with compensation for m = 0.3 are shown in Fig.18b), respectively. Further results for m = 0.8 without compensation are displayed in Fig. 19(a), respectively. The second-order harmonic was reduced by compensation to a negligible value of around 0.3% in the diagram of the FFT of the load current, as shown in Fig. 19(b). The algorithm was ultimately verified with two different dc capacitors with capacitances of $C_1 = 4700\ \mu F$ and $C_2 = 220\,\mu F$. Because of the low capacitance, the dc voltage on this capacitor had a considerably high ripple and its dc voltage varied between 48V and 64V, while the dc voltage on the second capacitor was held approximately smooth at 70V. The different capacitors produced different dc sources, which in turn caused asymmetrical output voltages/currents. The FFT diagram in Fig. 20(a) revealed a significant increase in the second-order harmonics.

With compensation: After applying the compensating algorithm, the spectrum of the load current was improved, as shown in Fig. 20(b). Under the same conditions, the FFT diagram of the load current with the compensating algorithm revealed that the second harmonic content of 1.26% for the uncompensated algorithm had been reduced to a negligible value for the compensating algorithm. As a result, the outputs regained their balance.

Influence of the global offset at high modulation index: In other experiments with compensated outputs, the dc voltage sources were set as $v_{C1} = 100\text{ V}$, $v_{C2} = 80\text{ V}$, the RL load was $R = 10\,\text{W}$, L= 30mH and the switching frequency was 10kHz. The influence of the unbalanced dc sources on the voltage waveform for different CMV setting was demonstrated in Fig.21. For instance, the offset for m = 0.866, in minimum CMV PWM had to be set to an extreme value and the control was turned into a discontinuous PWM mode, while in the medium CMV PWM, the voltage diagram was always in the discontinuous PWM mode irrespective of the change of the dc sources.

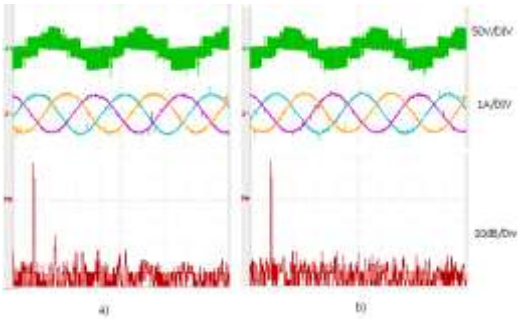

Fig. 18. Diagram of the phase load voltage, the load currents and the FFT of the load current (a) without compensation and (b) with compensation for m = 0**.3**

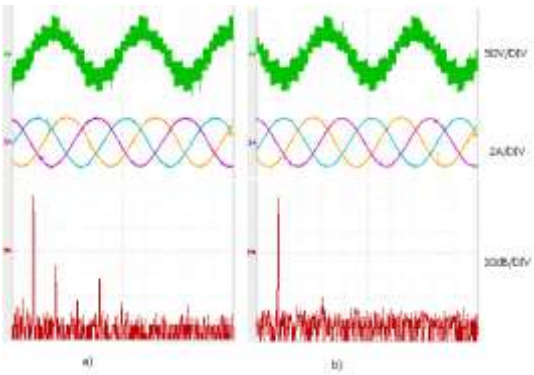

Fig. 19. Diagram of the phase load voltage, the load currents and the FFT of the load current (a) without compensation and (b) with compensation for m = 0.8.

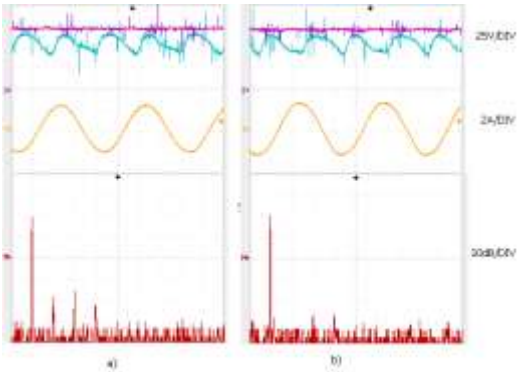

Fig. 20. Diagram of the dc sources and the output current for the algorithm (a) without compensation and (b) with compensation under a variable dc voltage: $C_1 = 220\,mF$, $C_2 = 4700\,mF$, $R = 10\,\text{W}$, L = 60 mH, $V_{c2} = 70$ V, and V_{c1} = variable (48-64 V).

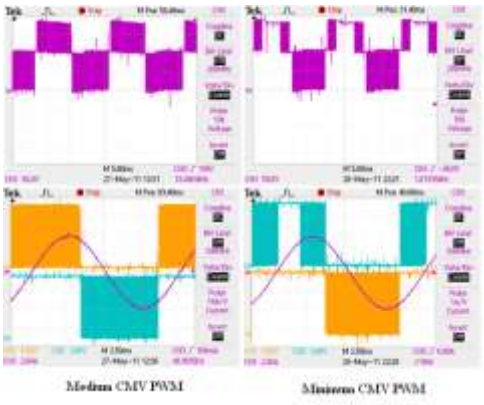

Fig.21. Diagrams of the phase to neutral point voltage [50V/div, 5ms/div], and trigger pulse versus load current [2A/div, 2.5ms/div] of a phase for m = 0.866 in the medium CMV PWM and the minimum CMV PWM methods**.**

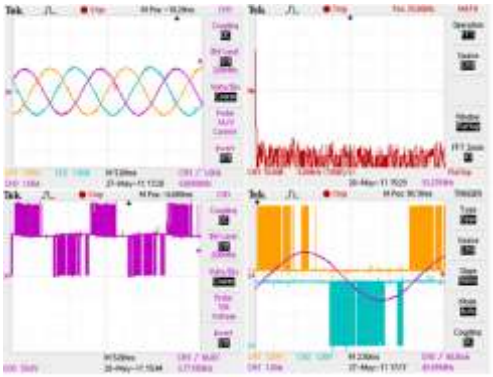

Fig.22: Diagrams of the load currents [1A/div, 5ms/div] and corresponding FFT [10dB/div, 5kHz/div], a phase to neutral point voltage [50V/div, 5ms/div] and trigger pulse versus load current [1A/div, 2.5ms/div] in the current based Discontinuous PWM for m = 0.3, and medium CMV**.**

Active switching voltage control for reduced switching loss: The effect of the local offset controller was demonstrated in medium CMV Discontinuous PWM mode as shown Figs.22 (m = 0.3) and Fig.23 (m = 0.866). The local offset was added to gain a DPWM mode depending on the phase load current values. The inverter leg appeared without commutation during the intervals that its corresponding load current attained a maximum or medium absolute value in compared with the two remaining phases. As a result of that current controlled DPWM mode, the switching loss can be significantly reduced, similar to the case of input voltage balance [25].

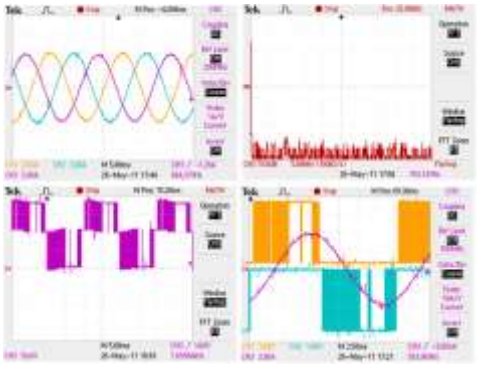

Fig.23. Diagrams of the load currents [2A/div, 5ms/div] and corresponding FFT [10dB/div, 5kHz/div], a phase to neutral point voltage [50V/div, 5ms/div] and trigger pulse versus load current [2A/div, 2.5ms/div] in the current based Discontinuous PWM for m=0.866 and medium CMV**.**

5. Conclusion

In this paper, the modeling of the switching voltages and the unified offset-based PWM scheme under the DC voltage imbalance was proposed. The PWM algorithm can be applied to both NPC and cascade multilevel inverter. In the scheme, the global offset allows to extend a maximized output voltage range in under-modulation range and define draft common mode voltage. The local offset can be flexibly modified in order to establish different PWM modes related to the switching loss and current ripple. The experimental results for the feed-forward compensating output voltages and for optimizing the switching loss in a DPWM mode under a DC voltage imbalance confirm the validity of the proposed PWM method.

References

[1] G. Carrara, S.Gardella, M. Marchesoni, R. Salutari, and G.Sciutto, ”A new multilevel PWM method- A theoretical analysis,” IEEE Trans. Power Electronics, Vol.7, pp.497-505 1992

[2] J.Rodríguez, J.S.Lai, and F. Z. Peng,”Multilevel Inverters: A Survey of Topologies, Controls, and Applications”, IEEE Transactions on Industrial Electronics, Vol. 49, No. 4, August 2002

[3] McGrath, B.P.; Holmes, D.G.; Lipo, T., “Optimized space vector switching sequences for multilevel inverters”, IEEE Transactions on Power Electronics, Vol.18, No.6, Nov.2003, pp.1293-1301

[4] N.V.Nho, M.J.Youn,”Comprehensive study on Space Vector PWM and carrier based PWM correlation in multilevel invertors”, IEE Proceedings Electric Power Applications , Vol.153, No.1, Jan 2006, pp.149-158

[5] S.B-Monge, J.Bordonau, D. Boroyevich, and S.Somavilla, ” The Nearest Three Virtual Space Vector PWM—A Modulation for the Comprehensive Neutral-Point Balancing in the Three-Level NPC Inverter”, IEEE Power Electronics Letters, Vol. 2, No. 1, March 2004 , pp.11-15

[6] N. Celanovic, and D. Boroyevich, “A fast space vector modulation algorithm for multilevel three phase converters,” IEEE Trans on Industry Applications, Vol.37, No.2, 2001, pp. 637-641.

[7] J. Rodriguez, P. Correa, and L. Moran, “A vector control technique for medium voltage multilevel inverters,” Applied Power Electronics Conference and Exposition(APEC), Vol.1, 2001, pp.173-178.

[8] Sanmin Wei and Bin Wu Fahai Li and Congwei Liu, “A General Space Vector PWM Control Algorithm for Multilevel Inverters”, Proceedings of the Applied Power Electronics Conference and Exposition, 2003., APEC '03.

[9] Ahmet M. Hava, Russel J. Kerkman, and Thomas A. Lipo ,”A High-Performance Generalized Discontinuous PWM Algorithm”, IEEE Transactions On Industry Applications, Vol. 34, No. 5, September/October 1998, pp. 1059-1071

[10] Blasko, V.: ‘A hybrid PWM strategy combining modified space vector and triangle comparison methods’. Proc. IEEE PESC Conf., 1996, pp.1872–1878

[11] C.B. Jacobina, A.M..N Lima , E.R.C. da Silva, R.N.C. Alves, and P.F. Seixas, “Digital Scalar Pulse-Width Modulation: A Simple Approach to Introduce Non-Sinusoidal Modulating Waveforms”, IEEE Transactions On Power Electronics, Vol. 16, No. 3, May 2001, pp. 351-359

[12] H. Van Der Broeck, H. Skudelny, and G. Stanke, “Analysis and realization of a pulse width modulator based on voltage space vectors,” in IEEE-IAS Conf. Rec., 1986, pp. 244–251.

[13] Keliang Zhou and Danwei Wang , “Relationship Between Space-Vector Modulation and Three-Phase Carrier-Based PWM: A Comprehensive Analysis”, IEEE Transactions On Industrial Electronics, Vol. 49, No. 1, February 2002, pp.186-196

[14] J. Pou,,D. Boroyevich, and R. Pindado, “Effects of Imbalances and Nonlinear Loads on the Voltage Balance of a Neutral-Point-Clamped Inverter”, EEE Transactions on Power Electronics, Vol. 20, No. 1, January 2005, pp. 123-131

[15] Josep Pou, Rafael Pindado, and Dushan Boroyevich,” Voltage-Balance Limits in Four-LevelDiode-Clamped Converters With Passive Front Ends”, IEEE Transactions On Industrial Electronics, Vol. 52, No. 1, February 2005, pp.190-196.

[16] K.Celanovic, D.Boroyevich,” A Comprehensive Study of Neutral-point voltage balancing problem in three-level voltage source PWM Inverters”, Transactions on Power Electronics, Vol.15, No.2, 2000, pp. .242-249

[17] P.C. Loh, D.G. Holmes, Y. Fukuta, and T.A. Lipo , “Reduced Common-Mode Modulation Strategies for Cascaded Multilevel Inverters”, IEEE Transactions On Industry Applications, Vo. 39, No. 5, September/October 2003, pp. 1386 -1395

[18] N.V.Nho, H.H. Lee,”Generalized Carrier PWM Algorithms For Multilevel Inverters With Unbalanced DC Voltages”, Proceeding of the 37th IEEE Power Electronics Specialists Conference PESC 18-22nd June 2006, Jeju , Korea.

[19] Kouro, S.; Lezana, P.; Angulo, M.; Rodriguez, J.; , "Multicarrier PWM With DC-Link Ripple Feedforward Compensation for Multilevel Inverters," Power Electronics, IEEE Transactions on , vol.23, no.1, pp.52-59, Jan. 2008

[20] N.V.Nho, H.H.Lee,"Carrier PWM Algorithm For Multi-leg Multilevel Inverters”, EPE 2007 - 12th European Conference on Power Electronics and Applications 2 - 5 September 2007, Aalborg, Denmark

[21] O. Lopez, J. Alvarez, J.I. Leon, J. Doval-Gandoy, F.D. Freijedo, “Multilevel Multiphase space vector PWM algorithm”, IEEE Transactions on Industrial Electronics, May 2008, Vol. 55, No. 5, pp.1933-1942

[22] J.I. Leon, S. Vazquez, J.A. Sanchez, R. Portillo, L.G. Franquelo, J.M. Carrasco, and E.Dominguez,” Conventional Space-Vector Modulation Techniques Versus the Single-Phase Modulator for Multilevel Converters”, IEEE Transactions on Industrial Electronics, July 2010, Vol. 57, No. 7, pp. 2473 – 2482

[23] J.I.Leon, Sergio Vazquez, Ramon Portillo, Leopoldo G. Franquelo, Juan M. Carrasco, Patrick W. Wheeler, and Alan J., “Three- Dimensional Feedforward Space Vector Modulation Applied to Multilevel Diode-Clamped Converters”, Industrial Electronics, IEEE Transactions on, Jan. 2009, Vol. 56, No. 1, pp.101-109

[24] N.V. Nho, Q.T. Hai and Hong-Hee Lee, " Carrier based Single-state PWM Technique Of Minimized Vector Error In Multilevel Inverter ", Journal of Power Electronics, Vol.10, No.4, July, 2010

[25] N.V. Nho, N.X. Bac and H-H. Lee, "An Optimized Discontinuous PWM Method to Minimize Switching Loss for Multilevel Inverters", IEEE Transactions On Industrial Electronics, 2011

[26] T. Brückner, and D.G. Holmes, “Optimal Pulse-Width Modulation for Three-Level Inverters”, IEEE Transactions On Power Electronics, Vol. 20, No. 1, January 2005, pp 82-89.

[27] K.A.Corzine, and J.R. Baker, “Multilevel Voltage-Source Duty-Cycle Modulation: Analysis and Implementation” IEEE Transactions On Industrial Electronics, Vol.. 49, No. 5, October 2002, pp.1009-1016

[28] F. Wang, “Sine-triangle versus space-vector modulation for three-level PWM voltage-source inverters,” IEEE Transactions On Industry Applications, Vol. 38, No. 2, Mar./Apr. 2002, pp. 500–506

[29] B.P. McGrath, D.G. Holmes, and T. Meynard, “Reduced PWM Harmonic Distortion for Multilevel Inverters Operating Over a Wide Modulation Range”, IEEE Transactions On Power Electronics, Vol. 21, No. 4, July 2006, pp. 941-949

[30] J. Pou, J. Zaragoza, S. Ceballos, M. Saeedifard, D. Boroyovich, “A Carrier based PWM strategy With Zero sequence Voltage Injection for a three-level Neutral Point Clamped Converter”, IEEE Transactions on Power Electronics, available online 2010.

[31] W. Chenchen, L. Yongdong, “Analysis and Calculation of Zero sequence voltage considering Neutral-point potential Balancing in Three-level NPC Converters”, IEEE Transactions On Industrial Electronics, Vol.57, No.7, July 2010, pp. 2262 - 2271

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